PATENT
Attorney Docket No. 401532/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HIROAKI TAMURA

Application No. Unassigned

Filed: January 14, 2002

For: SEMICONDUCTOR DEVICE

Art Unit: Unassigned

Examiner: Unassigned

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 4 with:

The present invention relates to a semiconductor device, such as an LSI, capable of repairing a memory by switching from a faulty portion in a memory to a memory for a redundant circuit which operates normally and omitting a test after performing such a repair.

Replace the paragraph beginning at page 1, line 11 with:

Conventionally, forming a redundant circuit in addition to and together with a main memory circuit in a semiconductor device is known. Such redundant circuit is formed in order to improve the yield in a fabricating process. The redundant circuit can be used in place of a part or all of the main memory circuit. An operation test (self test) to check whether the main memory circuit is operating normally is conducted during the fabricating process. If the operation test shows that the main memory circuit is defective, a portion in the main memory circuit that is defective is identified by an analysis for repair, and the redundant circuit is utilized in place of this portion. The redundant circuit is utilized in place of the defective portion of the main memory circuit generally as follows. As explained above, the

defective portion of the main memory circuit is known from the analysis for repair. Fuses are provided between the redundant circuit and a plurality of portions of the main memory circuit. The fuse(s) corresponding to the defective portion of the main memory circuit are blown using laser beams.

Replace the paragraph beginning at page 2, line 6 with:

Since such a redundant circuit is formed from the beginning, there is a disadvantage that an overall area of the semiconductor device increases, or the packing density increases. However, since the redundant circuit is very effective from the viewpoint of the yield, it can not be eliminated.

Replace the paragraph beginning at page 2, line 12 with:

Blowing of the fuse mentioned above is performed as follows. That is, the fuse is melted and evaporated using the heat of laser beams. It is however known that when a number of fuses are repeatedly irradiated with laser beams, damage may be caused to the underlying layer(s) of the fuse. When a semiconductor device is formed in a position directly below a fuse, the semiconductor device is damaged by the irradiation of the laser beam, and the whole product becomes defective. Consequently, as shown in Fig. 5, a conventional semiconductor device 1 employs the following configuration. Regions of a circuit 2 for a general logic, various memories 3a and 3b including a redundant circuit for improving the yield, and a BIST (Built-In-Self-Test) circuit 4 for a memory test and, in addition, regions of fuses 5 are disposed together. No circuit element is disposed under the regions of the fuses 5. Even if a fuse is blown using heat, the heat will not cause an unnecessary damage because there is no circuit element under the fuses 5.

Replace the paragraph beginning at page 3, line 6 with:

In the conventional semiconductor device as described above, however, burning of a fuse with a laser beam at the time of replacing a main memory circuit with a redundant circuit is performed in the fabricating process. That is, a defect in the main memory circuit can be repaired only in the state of the wafer, and a failure in the circuit which occurs after the circuit is packaged cannot be addressed, so that the yield is low. The fuse is physically burnt. Consequently, once a fuse is burnt, the state is fixed and a defect which occurs later cannot be repaired. Thus, the yield is similarly low. Further, after a defect is repaired by burning a fuse with a laser beam, in order to confirm that a portion which cannot be repaired or an

insufficient repaired portion does not exist, screening of a failure to be repaired has to be performed, and cost for conducting a test for this purpose increases.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory having a redundant circuit; and

a substrate on which said first chip and second chip are mounted, wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory.

2. (Amended) The semiconductor device according to claim 1, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, and

said nonvolatile memory of said second chip stores,

a test program for detecting whether there is a faulty portion in said memory of said second chip

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

4. (Amended) The semiconductor device according to claim 1, further comprising a third chip, said third chip being mounted on said substrate, said third chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said third chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

7. (Amended) The semiconductor device according to claim 4, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

8. (Amended) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory;

a third chip having a redundant circuit; and

a substrate on which said first chip, said second chip, and said third chip are mounted, wherein information required for utilizing said redundant circuit on said third chip in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit of said third chip is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

9. (Amended) The semiconductor device according to claim 5, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

11. (Amended) The semiconductor device according to claim 8, further comprising a fourth chip, said fourth chip being mounted on said substrate, said fourth chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said fourth chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

13. (Amended) The semiconductor device according to claim 8, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

IN THE ABSTRACT:

Replace the Abstract with:

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes a first chip having an electrically rewritable nonvolatile memory and a second chip having memories including a redundant circuit for repair. The first and second chips are provided on a substrate. Information required for utilizing the redundant circuit in place of a faulty portion in the memory of the second chip is stored in the nonvolatile memory on the first chip. When a faulty portion is detected in the memory of the second chip, the redundant circuit is utilized in place of the faulty portion based on the information stored in the nonvolatile memory.

REMARKS

The foregoing Amendment corrects translational errors and conforms the claims to United States practice. No new matter is added.

Respectfully submitted,

LEYDIG, VOIT & MAYER, LTD.

Jeffrey A. Wyand
Registration No. 29,458

Suite 300
700 Thirteenth Street, N.W.
Washington, D.C. 20005
Telephone: (202) 737-6770
Facsimile: (202) 737-6776

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JAW:ves

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AMENDMENTS TO SPECIFICATION, CLAIMS AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 4:

The present invention relates to a semiconductor device, such as an LSI, capable of repairing a memory by ~~changing over~~ switching from a faulty portion in a memory to a memory for a redundant circuit which operates normally and omitting a test after performing such a repair.

Amendments to the paragraph beginning at page 1, line 11:

Conventionally, forming a redundant circuit in addition to and together with a main memory circuit in a semiconductor device is known. Such redundant circuit is formed in order to improve the yield in a fabricating process ~~is known~~. The redundant circuit can be used in place of a part or ~~entire~~ all of the main memory circuit. An operation test (self test) to check whether the main memory circuit is operating normally is conducted during the fabricating process. If the operation test shows that the main memory circuit is defective, a portion in the main memory circuit that is defective is ~~decided~~ identified by an analysis for repair, and the redundant circuit is utilized in place of this portion. The redundant circuit is utilized in place of the defective portion of the main memory circuit generally as follows. As explained above, the defective portion of the main memory circuit is ~~know~~ known from the analysis for repair. Fuses are provided between the redundant circuit and a plurality of portions of the main memory circuit. The fuse(s) corresponding to the defective portion of the main memory circuit are blown using laser beams.

Amendments to the paragraph beginning at page 2, line 6:

Since such a redundant circuit is formed from the beginning, there is a disadvantage that an overall area of the semiconductor device increases, or the packing density increases. However, since the redundant circuit is very effective from the viewpoint of the yield, it can not be eliminated.

Amendments to the paragraph beginning at page 2, line 12:

Blowing of the fuse mentioned above is performed as follows. That is, the fuse is melted and evaporated using the heat of laser beams. It is however known that when a number of fuses are repeatedly irradiated with laser beams, ~~a~~ damage may be caused to the underlying layer(s) of the fuse. When a semiconductor ~~electric~~ device is formed in a position directly below a fuse, the semiconductor ~~electric~~ device is damaged by the irradiation of the laser beam, and the whole product becomes defective. Consequently, as shown in Fig. 5, a conventional semiconductor device 1 employs the following configuration. Regions of a circuit 2 for a general logic, various memories 3a and 3b including a redundant circuit for improving the yield, and a BIST (Built-In-Self-Test) circuit 4 for a memory test and, in addition, regions of fuses 5 are disposed together. No circuit element is ~~not~~ disposed under the regions of the fuses 5. Even if a fuse is blown using heat, the heat will not ~~case~~ cause an unnecessary damage because there is no circuit element under the fuses 5.

Amendments to the paragraph beginning at page 3, line 6:

In the conventional semiconductor device as described above, however, burning of a fuse with a laser beam at the time of replacing a main memory circuit with a redundant circuit is performed in the fabricating process. That is, a defect in the main memory circuit can be repaired only in the state of the wafer, and a failure in the circuit which occurs after the circuit is packaged cannot be addressed, so that the yield is low. The fuse is ~~physical~~ physically burnt. Consequently, once a fuse is burnt, the state is fixed and ~~there is a case that~~ a defect which occurs later cannot be repaired. Thus, the yield is similarly low. Further, after a defect is repaired by burning a fuse with a laser beam, in order to confirm that a portion which cannot be repaired or an insufficient repaired portion does not exist, screening of a failure to be repaired has to be performed, and ~~a~~ cost for conducting a test for this purpose increases.

Amendments to existing claims:

1. (Amended) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory~~;~~,

a second chip including a memory having ~~therein~~ a redundant circuit~~;~~, and

a substrate on which said first chip and second chip are mounted, wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory ~~on~~ of said second chip is stored in said nonvolatile memory ~~on~~ of said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory.

2. (Amended) The semiconductor device according to claim 1, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, ~~wherein~~ and

said nonvolatile memory of said second chip stores,

a test program for detecting whether ~~or not~~ there is a faulty portion in said memory ~~on~~ of said second chip~~;~~

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory ~~on~~ of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion~~;~~, and

a software repair program for writing information required for utilizing the ~~determined~~ portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory ~~on~~ of said first chip.

4. (Amended) The semiconductor device according to claim 1, further comprising a third chip, said third chip being mounted on said substrate, said third chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said third chip stores,

a test program for detecting whether ~~or not~~ there is a faulty portion in said memory on said second chip~~;~~,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory ~~on~~ of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion~~;~~, and

a software repair program for writing information required for utilizing the ~~determined~~ portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory ~~on~~ of said first chip.

7. (Amended) The semiconductor device according to claim 4, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

8. (Amended) A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory;

a third chip having a redundant circuit; and

a substrate on which said first chip, said second chip, and said third chip are mounted, wherein information required for utilizing said redundant circuit on said third chip in place of a faulty portion in said memory ~~on~~ of said second chip is stored in said nonvolatile memory ~~on~~ of said first chip, and said redundant circuit ~~on~~ of said third chip is utilized in place of the faulty portion in said memory ~~on~~ of said second chip based on the information stored in said nonvolatile memory ~~on~~ of said first chip.

9. (Amended) The semiconductor device according to claim 5, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores,

a test program for detecting whether ~~or not~~ there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory ~~on~~ of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the ~~determined~~ portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory ~~on~~ of said first chip.

11. (Amended) The semiconductor device according to claim 8, further comprising a fourth chip, said fourth chip being mounted on said substrate, said fourth chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said fourth chip stores,

a test program for detecting whether ~~or not~~ there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory ~~on~~ of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the ~~determined~~ portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory ~~on~~ of said first chip.

13. (Amended) The semiconductor device according to claim 8, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

~~The~~A semiconductor device includes a first chip having an electrically rewritable nonvolatile memory and a second chip having memories including a redundant circuit for repair. The first and second chips are provided on a substrate. Information required for utilizing the redundant circuit in place of a faulty portion in the ~~memories on~~ memory of the second chip is stored in the nonvolatile memory on the first chip. When a faulty portion is detected in the ~~memories on~~ memory of the second chip, the redundant circuit is utilized in place of the faulty portion based on the information stored in the nonvolatile memory.

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PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory having a redundant circuit; and

a substrate on which said first chip and second chip are mounted, wherein information required for utilizing said redundant circuit in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit is utilized in place of the faulty portion in said memory on said second chip based on the information stored in said nonvolatile memory.

2. The semiconductor device according to claim 1, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, and

said nonvolatile memory of said second chip stores,

a test program for detecting whether there is a faulty portion in said memory of said second chip

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

3. The semiconductor device according to claim 2, wherein said nonvolatile memory in said circuit for memory test is rewritable.

4. The semiconductor device according to claim 1, further comprising a third chip, said third chip being mounted on said substrate, said third chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said third chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

5. The semiconductor device according to claim 4, wherein said nonvolatile memory in said circuit for memory test is rewritable.

6. The semiconductor device according to claim 1, wherein said first chip and second chip are stacked on said substrate.

7. The semiconductor device according to claim 4, wherein said first chip, said second chip, and said third chip are stacked on said substrate.

8. A semiconductor device comprising:

a first chip having an electrically rewritable nonvolatile memory;

a second chip including a memory;

a third chip having a redundant circuit; and

a substrate on which said first chip, said second chip, and said third chip are mounted, wherein information required for utilizing said redundant circuit on said third chip in place of a faulty portion in said memory of said second chip is stored in said nonvolatile memory of said first chip, and said redundant circuit of said third chip is utilized in place of the faulty portion in said memory of said second chip based on the information stored in said nonvolatile memory of said first chip.

9. The semiconductor device according to claim 5, wherein

said second chip further comprises a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory of said second chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

10. The semiconductor device according to claim 9, wherein said nonvolatile memory in said circuit for memory test is rewritable.

11. The semiconductor device according to claim 8, further comprising a fourth chip, said fourth chip being mounted on said substrate, said fourth chip including a circuit for memory test having a nonvolatile memory, wherein said nonvolatile memory on said fourth chip stores,

a test program for detecting whether there is a faulty portion in said memory on said second chip,

a repair analysis program for identifying the faulty portion when the test program detects that there is a faulty portion in said memory of said second chip, and determining a position of a portion in said redundant circuit that is to be utilized in place of the faulty portion, and

a software repair program for writing information required for utilizing the portion determined in said redundant circuit in place of the faulty portion identified by the repair analysis program in said nonvolatile memory of said first chip.

12. The semiconductor device according to claim 11, wherein said nonvolatile memory in said circuit for memory test is rewritable.

13. The semiconductor device according to claim 8, wherein said first chip, said second chip, and said third chip are stacked on said substrate.